REMARKS

This is in response to the Office Action mailed on July 15, 2004, and the references cited therewith.

Claims 1, 3-4, 7, 17, 19, 21 and 23-26 are amended, as a result claims 1-26 are now pending in this application.

In the office action, the examiner objected to the phrase "said signal" in claim 25. This phrase has been changed to "a signal on the external control line" as suggested by the examiner.

§103 Rejection of the Claims

Claims 1, 2, 5-7, 9, 13 and 20 were rejected under 35 USC § 103(a) as being unpatentable over Chu et al. (U.S. Patent No. 4,785,393) in view of Narita et al. (U.S. Patent No. 5,293,558).

We respectfully traverse this rejection.

As the examiner acknowledges, in the system described by Chu et al, the data register and the shifter that are connected to the output of the ALU have a data width corresponding to the data width of the ALU output. In the specific embodiment described, that data width is 32 bits. The examiner contends that Narita discloses the missing elements from Chu. We respectfully disagree. Whilst the width of the shifter and data register in Narita is "2n", this is also the width of the output of the ALU. In this regard, see column 9 lines 65 to 68. In particular, this sentence states that the ALU carries out 2n arithmetic and/or logic operations on data taken in from the bus 14 or data output by the variable shifter 15 and outputs the results to the 2n bit wide bus 14. It is clear, therefore, that Narita discloses no more than Chu in that the width of the data register and the shifter are the same as the width of the ALU output.

In contrast, the claimed invention requires a wide data register and a shifting circuit of width substantially greater than n bits, where n is the width of the input and output data paths of

the common arithmetic unit. Therefore, even if those skilled in the art had decided to combine the teachings of Chu with Narita, they would still not have arrived at the claimed invention.

With regard to the sixty-four bit shifter 126 described by Chu et al, this shifter is provided for a completely different function, has a different structure to the claimed shifter and is not provided at the output of the arithmetic unit. Further, it only has a thirty-two bit output and cannot, therefore, be used for multiplication operations involving its two thirty-two bit inputs. Therefore, nothing in Chu et al discloses or suggests the claimed invention.

We therefore submit that the invention claimed in claim 1 is both novel and inventive over the cited art. We also submit that dependent claims 2 to 26 are also in an allowable format at least because they depend from an allowable main claim.

Allowable Subject Matter

Claims 3, 4, 8, 10-12, 14-19 and 21-26 were objected to as being dependent upon a rejected base claim, but were indicated to be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance, and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 349-9592 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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Date Nov. 15, 2004

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: ~~MS Amendment~~, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 15th day of November, 2004.

PATRICIA A. HULTMAN

Name

Signature